AMENDED CLAIMS

[Received by the International Office on December 28, 2004 (12.28.04), original claims 1-16 replaced by amended claims 1-9]

1. A digital-analog converter having:
(a) an array arrangement (22) having a number of cells (23) between a first and a last cell for outputting at least one quantized analog signal (25, 25') on the basis of control signals (17, 17', 18, 18', 19, 19', 20, 20', 21, 21');

(b) a DEM logic device (10) for generating at least one arithmetic sign signal (15) and two digital output data items (13, 14) from digital input data (11) on the basis of a predetermined algorithm in order to determine an initial cell and a final cell in the array arrangement (22), between which there are situated cells (24) having energy sources (30) which are to be activated, the arithmetic sign signal (15) determining whether cells adjoining the first cell in the array arrangement (22) are activated if the cells (24) to be activated reach the last cell in the array arrangement (22), and having

(c) a decoder device (16) for decoding the at least two digital output data items (13, 14) and the arithmetic sign signal (15) from the DEM device (10) into actuation signals (17, 17', 18, 18', 19, 19', 20, 20', 21, 21') in order to activate the cells (24) which are to be activated.

2. The digital-analog converter as claimed in claim 1,
wherein
the array arrangement (22) has single cells (23) with a

respective current source as energy source (30).

3. The digital-analog converter as claimed in claim 1 or 2,
wherein
the DEM logic device (10) has a parallel input for supplying the digital input data (11), which have a predetermined bit length.

4. The digital-analog converter as claimed in one of the preceding claims,
wherein
the output of the decoder device (16) has two row actuation signals (18, 20) and three column actuation signals (17, 19, 21) and preferably two associated complementary row actuation signals (18', 20') and three complementary column actuation signals (17', 19', 21') which are coupled to the array arrangement (22) for the purpose of activating energy sources (30) for predetermined cells (24).

5. The digital-analog converter as claimed in one of the preceding claims,
wherein
the array arrangement (22) has two mutually inverse quantized analog output signals (25, 25').

6. The digital-analog converter as claimed in one of the preceding claims,
wherein
the array arrangement (22) has single cells (23) with a respective local decoder device (27) whose input respectively has two row actuation signals (18, 20) and three column actuation signals (17, 19, 21) and preferably two associated complementary row actuation signals (18', 20') and three complementary column actuation signals (17', 19', 21').

7. The digital-analog converter as claimed in claim 6,
wherein
the local decoder device (27) respectively connects an energy source (30) to a resistor (31) when a first column signal (17) and a first row signal (18), or a second column signal (19) and a second row signal (20), or a third column signal (21), are activated.

8. The digital-analog converter as claimed in one of the preceding claims,
wherein
the array arrangement (22) has a respective edge length of at least 64 cells (23), corresponding to a bit length for the input signal of at least 12 bits.

9. The digital-analog converter as claimed in one of the preceding claims,
wherein
a DWA (Data Weighted Averaging) algorithm or a bi-DWA (bidirectional Data Weighted Averaging) algorithm or an ILA (Individual Level Averaging) algorithm is used in the DEM logic device (10) in order to determine the cells (24) in the array arrangement (22) which are to be activated.